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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/718,493	11/20/2003	Bruno Pellat	02GR220554486	8225

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EXAMINER	
HAROON, ADEEL	

ART UNIT	PAPER NUMBER
2685	

DATE MAILED: 03/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/718,493	PELLAT ET AL.	
	Examiner	Art Unit	
	Adeel Haroon	2685	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 15, 16, 18, 22, 24, 28, 29, 31, 38, 39, 40, 42, and 46 are rejected under 35 U.S.C. 102(e) as being anticipated by Khorram (U.S. 6,970,689).

With respect to claims 15 and 22, Khorram discloses a process for reducing nonlinearities of a frequency transposition device. Khorram discloses inactivating the local oscillator in a calibration mode in step 1606 (Column 12, line 65 – Column 13, line 1). Khorram discloses calibrating in succession two differential pairs of transistors by setting to zero a reference path current with elements134, 142, 170, and 172 of one of the pairs of transistors not undergoing calibration and setting a voltage difference applied to the control terminals of the other pair of transistors undergoing calibration until an output voltage of the mixer is set to zero within a predetermined accuracy

(Column 9, lines 1-28). Khorram also discloses storing the voltage difference applied to the control terminals of the two differential pairs of transistors after calibration (Column 13, lines 54-58). Khorram further discloses activating the local oscillator in a normal mode for deactivating the calibration loop, and applying the stored voltage differences to the respective control terminals of the transistors (Column 13, lines 11-17).

With respect to claim 16, Khorram shows the two differential pairs of transistors as being statically mutually disconnected and dynamically mutually connected in figure 6.

With respect to claims 18 and 24, Khorram shows the reference path, the path after 170 and 172, corresponds to ground.

With respect to claim 28, Khorram discloses a frequency transposition device including a local oscillator for providing a local oscillator signal, LO (Column 8, lines 64-67). Khorram also discloses current switching circuit comprising two differential pairs of transistors, 152, 154, 162, and 164, controlled by the local oscillator signal and with a control terminal (Column 8, lines 55-63). Khorram discloses a calibration loop for calibrating the transistors in succession two differential pairs of transistors by setting to zero a reference path current with elements134, 142, 170, and 172 of one of the pairs of transistors not undergoing calibration and setting a voltage difference applied to the control terminals of the other pair of transistors undergoing calibration until an output voltage of the mixer is set to zero within a predetermined accuracy (Column 9, lines 1-28). Khorram also discloses a storage circuit for storing the voltage difference applied to the control terminals of the two differential pairs of transistors after calibration

(Column 13, lines 54-58). Khorram discloses inactivating the local oscillator in a calibration mode in step 1606 (Column 12, line 65 – Column 13, line 1). Khorram further discloses activating the local oscillator in a normal mode for deactivating the calibration loop, and applying the stored voltage differences to the respective control terminals of the transistors (Column 13, lines 11-17).

With respect to claim 29, Khorram shows the two differential pairs of transistors as being statically mutually disconnected and dynamically mutually connected in figure 6.

With respect to claims 31, Khorram shows the reference path, the path after 170 and 172, corresponds to ground.

With respect to claim 38, Khorram discloses that the device is an integrated circuit (Column 11, lines 2-5).

With respect to claim 39, Khorram discloses a cellular phone with a RF stage including a local oscillator for providing a local oscillator signal, LO (Column 8, lines 64-67). Khorram also discloses current switching circuit comprising two differential pairs of transistors, 152, 154, 162, and 164, controlled by the local oscillator signal and with a control terminal (Column 8, lines 55-63). Khorram discloses a calibration loop for calibrating the transistors in succession two differential pairs of transistors by setting to zero a reference path current with elements134, 142, 170, and 172 of one of the pairs of transistors not undergoing calibration and setting a voltage difference applied to the control terminals of the other pair of transistors undergoing calibration until an output voltage of the mixer is set to zero within a predetermined accuracy (Column 9, lines 1-

28). Khorram discloses inactivating the local oscillator in a calibration mode in step 1606 (Column 12, line 65 – Column 13, line 1). Khorram further discloses activating the local oscillator in a normal mode and applying the voltage differences to the respective control terminals of the transistors (Column 13, lines 11-17).

With respect to claim 40, Khorram also discloses a storage circuit for storing the voltage difference applied to the control terminals of the two differential pairs of transistors after calibration (Column 13, lines 54-58).

With respect to claims 42, Khorram shows the reference path, the path after 170 and 172, corresponds to ground.

With respect to claim 46, Khorram teaches the mixer to compensate for temperature variations (Column 13, lines 61-64).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 17, 23, 30, 37, 41, and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Khorram in view of Murtojarvi et al. (U.S. 6,393,260).

With respect to claims 17 and 23, the process of Khorram is described above in the discussion of claims 15 and 22. Khorram does not expressly disclose that the transistors are bipolar and the control terminals correspond to the bases of the transistors. However, Murtojarvi et al. disclose a process for attenuating nonlinearities in a mixer by adjusting the voltage difference in a pair of transistors thus making it analogous art since it is in the same field of endeavor. Murtojarvi et al. also disclose two differential pairs of bipolar transistors (Column 6, lines 43-45). Murtojarvi et al. further teach that the control terminals, BLO+ and BLO-, which control voltage difference, correspond to bases of the bipolar transistors (Column 4, lines 41-47). Therefore, it would be obvious to one of ordinary skill in the art at the time of the applicant's invention to apply the control terminals that correspond to the bases of bipolar transistors as taught by Murtojarvi et al. in the process of Khorram in order to attenuate even-order spurious signals.

With respect to claims 30 and 41, the device of Khorram is described above in the discussion of claims 28 and 39. Khorram does not expressly disclose that the transistors are bipolar and the control terminals correspond to the bases of the transistors. However, Murtojarvi et al. disclose a process for attenuating nonlinearities in a mixer by adjusting the voltage difference in a pair of transistors thus making it analogous art since it is in the same field of endeavor. Murtojarvi et al. also disclose two differential pairs of bipolar transistors (Column 6, lines 43-45). Murtojarvi et al. further teach that the control terminals, BLO+ and BLO-, which control voltage difference, correspond to bases of the bipolar transistors (Column 4, lines 41-47).

Therefore, it would be obvious to one of ordinary skill in the art at the time of the applicant's invention to apply the control terminals that correspond to the bases of bipolar transistors as taught by Murtojarvi et al. in the process of Khorram in order to attenuate even-order spurious signals.

With respect to claims 37 and 48, the device of Khorram is described above in the discussion of claims 28 and 39. Khorram does not expressly disclose capacitors connected to the transistors. However, Murtojarvi et al. disclose a process for attenuating nonlinearities in a mixer by adjusting the voltage difference in a pair of transistors thus making it analogous art since it is in the same field of endeavor. Murtojarvi et al. also disclose capacitors, C1 and C2, connected in series wherein the control terminals of each pair of transistors are coupled to said pair of capacitors. Therefore, it would be obvious to one of ordinary skill in the art at the time of the applicant's invention to include Murtojarvi et al.'s capacitors in the device of Khorram in order to produce bias current and voltages.

5. Claims 19-21, 25-27, 32-36, 43-45, and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Khorram in view of Redman-White (U.S. 2004/0017862).

With respect to claims 19 and 25, the process of Khorram is described above in the discussion of claims 15 and 22. Khorram does not expressly disclose the method of detecting the voltage differences between the terminals. However, Redman-White disclose adjusting the bias to reduce nonlinearities in a mixer by adjusting the voltage

difference in a pair of transistors thus making it analogous art since it is in the same field of endeavor. Redman-White disclose detecting the outputs of the two pairs of transistors in figure 3 (Paragraphs 20 and 21), which would entail detecting a change in sign of a difference in the output voltage. Therefore, it would be obvious to one of ordinary skill in the art at the time of the applicant's invention to apply the difference voltage detecting technique as taught by Redman-White in the process of Khorram in order to have a more comprehensive voltage detection system.

With respect to claims 20 and 26, Khorram discloses digital/analog converters, element number 1308, coupled to the control terminals of the transistors, where setting the differences comprise changing a digital control word, comparison result (Column 12, lines 4-24). Khorram further disclose storing the voltage difference after calibration (Column 13, lines 11-17).

With respect to claims 21 and 27, Khorram further discloses modifying the voltage difference until the outputs are matched, relating to the sign of the difference in the output voltage is detected (Column 9, lines 1-28).

With respect to claims 32, 33, 43, and 44, the device of Khorram is described above in the discussion of claim 28. Khorram does not expressly disclose the method of detecting the voltage differences between the terminals. However, Redman-White disclose adjusting the bias to reduce nonlinearities in a mixer by adjusting the voltage difference in a pair of transistors thus making it analogous art since it is in the same field of endeavor. Redman-White disclose detecting the outputs of the two pairs of transistors in figure 3 with a comparator having inputs coupled to the pair of differential

outputs (Paragraphs 20 and 21), which would entail detecting a change in sign of a difference in the output voltage. Therefore, it would be obvious to one of ordinary skill in the art at the time of the applicant's invention to apply the difference voltage detecting technique as taught by Redman-White in the process of Khorram in order to have a more comprehensive voltage detection system.

With respect to claim 34 and 45, Khorram discloses digital/analog converters, element number 1308, coupled to the control terminals of the transistors, where setting the differences comprise changing a digital control word, comparison result (Column 12, lines 4-24). Khorram further disclose storing the voltage difference after calibration (Column 13, lines 11-17).

With respect to claim 35, Khorram teaches the mixer to compensate for temperature variations (Column 13, lines 61-64).

With respect to claims 36 and 47, Khorram teaches deactivating the calibration loop by deactivating the detection and monitoring circuit (Column 13, lines 11-26).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Sagawa et al. (U.S. 5,715,532) disclose a frequency converter that reduces nonlinearities by changing the base voltage of the transistors in the converter. Kramer (U.S. 6,763,227) discloses a calibration method of a modulator.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Adeel Haroon whose telephone number is (571) 272-7405. The examiner can normally be reached on Monday thru Friday, 8:30 a.m. - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nay Maung can be reached on (571) 272-7882. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AH
2/27/06

Nguyen Vo
3-1-2006

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PRIMARY EXAMINER